ABSTRACT

An integrated circuit is provided for scan driving that can significantly reduce the chip size. In first region AODD, odd-numbered output pads OUT1, OUT3, ... OUT173, OUT175, driver circuits DR1, DR3,... DR173, DR175, and flip-flops SREG1, SREG3, ... SREG173, SREG175 in an order corresponding to the order of the odd-numbered scanning lines are each arranged as a column in the X-direction, and, at the same time, output pads OUTi, driver circuits DRi and flip-flops SREGi corresponding to the scanning lines are arranged in the same row in the Y-direction (chip width direction). In second region AEVEN, even-numbered output pads OUT2, OUT4, ... OUT174, OUT176, driver circuits DR2, DR4,... DR174, DR176, and flip-flops SREG2, SREG4, ... SREG174, SREG176 in an order corresponding to the order of the even-numbered scanning lines are each arranged as a column in the X-direction, and, at the same time, output pads OUTi, driver circuits DRi and flip-flops SREGi corresponding to the scanning lines are arranged in the same row in the Y-direction (chip width direction).